SPECIFICATION

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, more specifically, it relates to a semiconductor device with a plurality of semiconductor chips stacked.

2. Detailed Description of the Related Art

FIG. 7 shows a conventional semiconductor device with a plurality of semiconductor chips 2,3 stacked on a substrate 1. As a high density mounting technique, a technique of laminating and mounting a plurality of semiconductor chips on a substrate, called stack mounting is used.

In the stack mounting, in general, the substrate and the stacked semiconductor chips are connected by wire bonding. Therefore, the semiconductor chips are stacked from one with a larger chip size so as to prevent interference of a semiconductor chip stacked above with a bonding pad of a semiconductor chip disposed below.

Since the bonding pad on the substrate is provided around the semiconductor chip in the lowermost layer, the upper layer semiconductor chip with a smaller chip size has a longer distance with respect to the bonding pad on the substrate. Therefore, with a larger chip size difference in the upper layer and the lower layer, the distance between the bonding pad of the upper layer semiconductor chip and the bonding pad on the substrate becomes longer. In particular,

in the case a wire per one loop becomes longer, the wire strength is lowered so that a trouble of sagging of the wire by its self weight, tilting of the wire at the time of sealing, or the like is generated so as to deteriorate the yield, and thus it is problematic.

FIG. 8 is a cross-sectional view of a semiconductor device disclosed in the unexamined Japanese Utility Model Publication (KOKAI) No. 2-146436.

The semiconductor device shown in FIG. 8 is a hybrid IC with IC chips stacked in two stages with the IC chips butted with each other and connected by a solder bump, wherein only the lower chip 20 is wire bonded, because the lower IC chip 20 is formed larger than the upper IC chip 30. However, according to the semiconductor device shown in FIG. 8, a problem is involved in that the lower semiconductor chip 20 should be provided with a pad matching with the upper semiconductor chip 30, and further, the lower semiconductor chip 20 should be a dedicated semiconductor chip to serve as a pair with the upper semiconductor chip 30.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a novel semiconductor device with an improved yield by solving the problems in the above-mentioned conventional technology, in particular, by shortening the wire length per one loop so as to eliminate the problems of wire sagging by its self weight, tilting of the wire at the time of sealing, or the like.

In order to achieve the above-mentioned object, the

present invention basically adopts the technological configurations described below.

That is, a first aspect of the present invention is a semiconductor device with a plurality of semiconductor chips stacked on a substrate, wherein the semiconductor device comprising; a wiring layer disposed so as to be sandwiched between the semiconductor chips, and a plurality of bonding pads, for connecting a bonding wire, provided on the wiring layer, thereto.

In the second aspect of the present invention, a connection wiring for connecting the bonding pads is provided in the wiring layer.

In the third aspect of the present invention, a plurality of bonding pads are disposed so as to surround a semiconductor chip stacked on an upper surface of the wiring layer.

In the fourth aspect of the present invention, a via hole is provided in the wiring layer, this via hole is connected to a bonding pad of a semiconductor chip disposed below the wiring layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view showing a first embodiment of a semiconductor device according to the present invention;

FIG. 2 is a cross-sectional view showing a second embodiment of a semiconductor device according to the present invention;

FIG. 3 is a cross-sectional view showing a third

embodiment of a semiconductor device according to the present invention;

FIG. 4 is a cross-sectional view showing a modified embodiment of the second embodiment;

FIG. 5 is a cross-sectional view showing a fourth embodiment of a semiconductor device according to the present invention;

FIG. 6 is a cross-sectional view showing a modified embodiment of the fourth embodiment;

FIG. 7 is a cross-sectional view showing a conventional embodiment; and

FIG. 8 is a cross-sectional view showing another conventional embodiment.

DESCRIPTION OF PREFERRED EMBODIMENTS

Hereinafter, embodiments of the semiconductor devices according to the present invention will be described in detail with reference to the drawings.

(First Embodiment)

FIG. 1 is a cross-sectional view showing a first embodiment of a semiconductor device according to the present invention. The semiconductor device shown in FIG. 1 has a plurality of semiconductor chips 2, 3 stacked on a substrate 1, wherein a wiring layer 7 is provided between the semiconductor chips 2, 3 for relaying wires 14a, 14b for wire bonding. Relaying bonding pads 71a, 71b are provided in the wiring layer 7.

Hereinafter, the first embodiment will be described in further detail.

In the first embodiment, the semiconductor chip 2 having an integrated circuit, a polyimide tape 7 with a copper foil layer interposed therein, and the semiconductor chip 3 having an integrated circuit are stacked and mounted by an adhesive 4 in this order on the printed wiring substrate 1 with a resin base material having an electric circuit of a copper wiring.

The printed wiring substrate 1, the semiconductor chip 2, and the semiconductor chip 3 each have bonding pads 11a to 11d, bonding pads 21a, 21b, and bonding pads 31a, 31b, capable of wire bonding for connection of the circuit stored in each thereof and an external circuit. Moreover, relaying pads 71a, 71b, connected to the copper foil layer, for wire bonding are provided in the polyimide tape 7.

A desired operation can be obtained by electrically connecting the circuits stored each in the printed wiring substrate 1, the semiconductor chip 2, and the semiconductor chip 3 with each other.

According to the semiconductor device with the configuration, the circuits stored in the printed wiring substrate 1 and the semiconductor chip 2 can be connected electrically by connecting the bonding pads 11b, 11c and the bonding pads 21a, 21b by wires 12a, 12b, respectively.

Similarly, the circuits stored in the printed wiring substrate 1 and the semiconductor chip 3 can be connected electrically by connecting the bonding pads 11a, 11d and the bonding pads 31a, 31b by wires 14a, 14b, respectively. In this case, the wires 14a, 14b are arranged from the bonding pads 31a, 31b of the semiconductor chip 3 for connection with

the relaying pads 71a, 71b of the polyimide tape 7, and further connection with the bonding pads 11a, 11d of the printed wiring substrate 1.

Wiring connection of three or more bonding pads like stepping stones is called stitching, which is a common technique of wire bonding.

(Second Embodiment)

FIG. 2 is a cross-sectional view showing a second embodiment of a semiconductor device according to the present invention. The semiconductor device shown in FIG. 2 has a wiring layer 7 provided with at least two relaying bonding pads 71a, 71b, and a connection wiring 72 for connecting the two relaying bonding pads 71a, 71b which are disposed so as to surround a semiconductor chip 3 stacked on the upper surface of the wiring layer 7.

Hereinafter, the second embodiment will be described in further detail.

The second embodiment comprises the semiconductor device shown in FIG. 1, wherein relaying pads 71a, 71b are connected electrically by a wiring 72 in the inner layer of a polyimide tape 7.

In the second embodiment, for example, a bonding pad 31a of the semiconductor chip 3 and a bonding pad 11d on a printed wiring substrate 1 on the opposite side with respect to the semiconductor chip 3 are connected via the inner layer wiring 72 of the polyimide tape 7. According to the configuration, in addition to the effects obtained by the first embodiment, the effect of improving the freedom in arranging the wiring between the printed wiring substrate 1

and the semiconductor chip 3 (in this case 73a, 14b) can be obtained.

(Third Embodiment)

FIGS. 3 and 4 are cross-sectional views showing a third embodiment of a semiconductor device according to the present invention. The semiconductor device shown in the figures has a wiring layer 8 provided with relaying bonding pads 81c, 81d, and via holes 82a, 82b connected with the relaying bonding pads 81c, 81d as well as formed through the wiring layer 8.

In the semiconductor device, the via holes 82a, 82b of the wiring layer 8 and bonding pads 21a, 21b of the semiconductor chip 2 provided below the wiring layer 8 are connected.

Hereinafter, the third embodiment will be described in further detail.

In the embodiment shown in FIG. 3, a wiring layer 8 formed by laminating polyimide and aluminum layers is provided on the semiconductor chip 2 instead of the polyimide tape 7.

According to the third embodiment, similar to the first embodiment, the relaying pads 81a to 81d are provided on the wiring layer 8 and the via holes 82a, 82b are provided on the wiring layer 8. The bonding pads 21a, 21b of the semiconductor chip 2 are connected to the via holes 82a, 82b so as to lead out the wirings of the bonding pads 21a, 21b to the surface of the wiring layer 8, respectively, and wirings 12a, 12b from the bonding pads 81c, 81d on the wiring layer 8 to the bonding pads 11b, 11c on the printed wiring substrate 1 are provided.

FIG. 4 shows an embodiment in which optional relaying

pads 81a and 81b are connected electrically by a wiring 83 provided in the inner layer of the wiring layer 8.

According to the configuration, in addition to the above-mentioned effects, freedom in arranging the wiring between the printed wiring substrate 1 and the semiconductor chip 3 can be improved.

(Fourth Embodiment)

FIGS. 5 and 6 are cross-sectional views showing a fourth embodiment of a semiconductor device according to the present invention.

FIG. 5 shows an embodiment with a semiconductor chip 2 provided as a cell base IC.

The cell base IC is a semi-custom LSI with a commonly used integrated circuit, such as a memory and a gate array, provided preliminarily in a semiconductor chip so that connection among circuits or connection with a bonding pad can be executed later according to the application. Since there is freedom in connecting the internal integrated circuit and the bonding pad, an unused bonding pad can be provided to some extent at an optional position. FIG. 5 shows an embodiment having the unused bonding pads 21a, 21b as a relaying pad. Compared with the embodiments shown in FIGS. 1 to 4, it has a simple configuration so that the effect of facilitating the assembly work can be provided.

FIG. 6 shows an embodiment in which optional unused bonding pads 21a, 21b of the semiconductor chip 2 are connected by a connection wiring 22 in the semiconductor device shown in FIG. 5. Also in this case, the effect of improving the arrangement of wiring between the printing

wiring substrate 1 and the semiconductor chip 3 can be obtained.

According to the semiconductor device of the present invention, owing to the above-mentioned configurations, since the wire length per one loop can be shortened, deterioration of the wire strength can be prevented, and thus the conventionally generated problems are eliminated so as to improve the yield.